A4000-060/040 XP Accelerator (Revs. 1 and 2)

(Digitally reconstructed by Greg Donner for quality/clarity) May 27, 1999

The new A4000-060/040 XP accelerator is a plugin board for the Amiga computer and is functionally compatible with the Amiga 4000T, Amiga 4000, and Amiga 3000 computers. New levels of performance and economy are achieved by integration of all programmable logic into one advanced "Complex Programmable Logic Device" (CPLD). Fewer components also means improved quality and reliability. Along with the performance and features offered on the original accelerator, the A4000-060/040 XP accelerator supports these additional enhancements.

Special technology makes it possible with EDO RAM to support zero "wait states" when in burst mode for both reads and writes to local memory. This improves memory access performance by over 40% when compared with standard RAM.

A new optional onboard SCSI-3 controller supporting Ultra/Wide SCSI-3 protocol provides synchronous data transfer rates of over 20 MB/sec. DMA access to CPU memory is over 80 MB/sec improving CPU overhead and SCSI latency. Included with the SCSI-3 controller is a new robust and optimized SCSI driver tested with a variety of SCSI-1, 2, and 3 devices.

Overall, the A4000-060/040 XP accelerator represents the most advanced accelerator for the Amiga to date while maintaining compatibility with existing software and a "price" the end-user can afford.

The A4000-060/040 XP accelerator is available for immediate delivery.

Specifications:

- Support for either 3.3V 68060 or 5V 68040 processors.
- Asynchronous support for CPU speeds of 33 to 66 MHz.
- 68060/040 Burst Mode supports zero "wait state" access for reads and writes to onboard memory.
- Optional Ultra/Wide SCSI-3 controller provides synchronous data transfer rates of over 20 MB/ sec. DMA access from SCSI controller to local memory is over 80 MB/sec.
- Four standard 72-pin SIMM sockets offering up to 128 MB of user-installable memory.
- Support for EDO (Extended Data Out) DRAMs for enhanced memory access.
- Support for 4 MB, 8 MB, 16 MB or 32 MB industry standard SIMMs with access time of 60 or 70ns.
- Optional Boot ROM socket for OS incompatibility fixes and/or SCSI driver.
- Support for Kickstart ROM mapping into Fast RAM for enhanced performance.
- IEEE floating-point library and instruction emulation software for support of the 68060 CPU and on-chip floating-point unit (FPU). This software includes fixes and enhancements for the 68060 CPU to insure optimum performance and compatibility with the Amiga's 3.1 Kickstart ROM (and later).
- Operating parameters: Ambient temperature = 0° C + 70° C, VCC = 5.0 volts 5% tolerance.

(Jumper Definitions on next page)

Jumper Definitions		
Jumper	Definition	Default
JP1	Reserved	OFF
JP2	Cache Burst to A4000 Motherboard	OFF
	CLOSED (ON) = Cache Burst Enabled OPEN (OFF) = Cache Burst Disabled	
JP3	Interrupt Pending, DMA Backoffs	OFF
	CLOSED (ON) = DMA Backoffs for Interrupt OPEN (OFF) = DMA Ignores Interrupt	
JP4	SCSI Option-1	OFF
	CLOSED (ON) = No LUN Support OPEN (OFF) = Support LUNs	
JP5	SCSI Option-2	OFF
	CLOSED (ON) = Autoboot Disabled OPEN (OFF) = Autoboot Enabled	
JP6	EPROM Type	1 and 2
	1 and 2 = $27C256$ 2 and 3 = $27C512$	
JP7	CPU Power	
	1 and 2 $(5V) = 68040$ 2 and 3 $(3.3V) = 68060$	
JP8	CPU Clock	
	1 and 2 = 68040 2 and 3 = 68060	
JR1	Fast Memory Write	OFF
	OPEN (OFF) = Fast Writes Enabled	
JR2	Memory Configured for Burst Mode	OFF
	OPEN (OFF) = Burst Mode Support (Two SIMMs Minimum Required) CLOSED (ON) = Non-Burst Mode (Support for any number of SIMMs)	

Jumper Definitions (continued)		
Jumper	Definition	Default
JR3	DRAM Speed vs. CPU Clock	OFF
	66MHz 50MHz 40MHz OPEN (OFF) = 50ns 60ns 60/70ns CLOSED (ON) = 60ns 60/70ns 60/70/80ns	
JR4	FCLK Option CLOSED (ON) => 58MHz	OFF
JR5	EDO DRAM Support OPEN (OFF) = EDO Enabled	OFF
JR6	Memory Size OPEN (OFF) = 4MB CLOSED (ON) = 16MB	OFF
JR7	Single/Double-Sided SIMM OPEN (OFF) = Single-Sided SIMM CLOSED (ON) = Double-Sided SIMM	OFF
JR8	On-Board SCSI Enable CLOSED (ON) = SCSI Enabled	OFF
CN5	According to Michael at GVP-m, these pins have no useful meaning for anybody but the manufacturer. They are simply the connection to the two large Programmable Logic Controller Chips, Altera EPX880 (or in older versions, EPX780). Via this connector, the Programmable Logic Controller chips on the accelerator are programmed "in system" after the boards were manufactured.	
CN6	5V Fan	
CN8	SCSI LED Indicator	